In the Abstract:

Please replace the Abstract with the following:

An integrated circuit wafer element and an improved method for bonding the same to produce a stacked integrated circuit. An integrated circuit wafer according to the present invention includes a substrate having first and second surfaces constructed from a wafer material, the first surface having a circuit layer that includes integrated circuit elements constructed thereon. A plurality of vias extend from the first surface through the circuit layer and terminate in the substrate at a first distance from the first surface. The vias include a stop layer located in the bottom of each via constructed from a stop material that is more resistant to chemical/mechanical polishing (CMP) than the wafer material. The vias may be filled with an electrically conducting material to provide vertical connections between the various circuit layers in a stacked integrated circuit.

A1

Please replace claim 1 with the following;

1. An integrated circuit wafer comprising:

a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon;

A2

a plurality of vias extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance between said first and second surfaces of said substrate, said vias having a bottom surface comprising a stop layer covering said bottom surface, said stop layer comprising a stop material that is more resistant to chemical/mechanical polishing (CMP) than said wafer material.

Please replace claim 7 with the following:

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